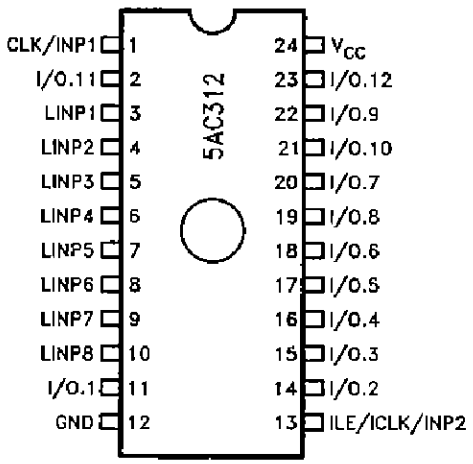
5AC312
1-MICRON CHMOS
ERASABLE PROGRAMMABLE
LOGIC DEVICE

- High-Performance LSI Semi-Custom Logic Alternative for Low-End Gate Arrays, TTL, and 74HC- or 74HCT SSI and MSI Logic, and PLDs
- High Speed tpd (max) 25 ns, 50 MHz Performance Pipelined, 33 MHz with Feedback
- 12 Macrocells with Programmable I/O Architecture; Up To 22 Inputs (10 Dedicated, 12 I/O)
- 8 Programmable Inputs Configurable as Latches, Registers or Flow-Through
- Programmable AND, Allocatable OR Design Allows up to 16 P-Terms per Macrocell
- Software-Supported P-Term Allocation between Adjacent Macrocells
- Programmable Output Registers Configurable as D, T, JK, or SR Types
- Dual Feedback on All Macrocells for Implementing Buried Registers with Bidirectional I/O
- 2 P-Terms on All Macrocell Control Signals
- Programmable Low-Power Option for Standby Operation; 100 μA Typical Standby Current
- UV Erasable (CerDIP) EPROM Technology or OTP
- 100% Generically Testable EPROM Logic Control Array
- Programmable Security Bit Allows 100% Protection of Proprietary Designs
- Available in 24-Pin 0.3″ CerDIP/PDIP and 28-Pin PLCC Packages
(See Packaging Spec., Order Number #231369)



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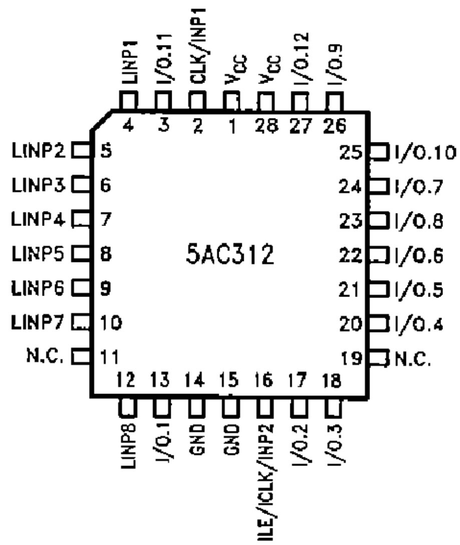

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Figure 1. Pin Configurations

October 1989
Order Number: 290156-003

INTRODUCTION

The Intel 5AC312 CHMOS EPLD (Erasable Programmable Logic Device) represents an innovative approach to overcoming the primary limitations of standard PLDs. Due to a proprietary I/O architecture and macrocell structure, the 5AC312 is capable of implementing high performance logic functions more effectively than previously possible. It can be used as an alternative to low-end gate arrays, multiple programmable logic devices or LS-, HC- or HCT SSI and MSI logic devices. Input and macrocell features for the 5AC312 are a superset of features offered by other PLD-type products.

The 5AC312 uses advanced CHMOS EPROM cells as logic control elements instead of poly-silicon fuses. This technology allows the 5AC312 to operate at levels necessary in high performance systems while significantly reducing the power consumption. Its programmable stand-by function reduces power consumption to almost "zero" in applications where a slight speed loss is traded for power savings.

ARCHITECTURE DESCRIPTION

The architecture of the 5AC312 is based on the familiar "Sum-Of-Products" programmable AND, fixed OR structure, though the 5AC312 macrocell contains a number of significant functional enhancements. This device can implement both combinational and sequential logic functions through a highly flexible macrocell and I/O structure. The 5AC312 has been designed to effectively implement both combinational-register and register-combinational-register forms of logic to easily accommodate state machine designs.

Figure 2 shows a global view of the 5AC312 architecture. The 5AC312 contains a total of 12 I/O macrocells, 8 user-programmable input structures, and 2 additional inputs that can be programmed to serve as either combinatorial inputs or clock inputs. Each of the eight inputs can be individually configured as a latch, register, or flow-through input. Input latches/registers can be synchronously or asynchronously clocked.

Each macrocell is further sub-divided into 16 Product Terms with 8 Product Terms dedicated to the control signals OE, PRESET, ASYNCH. CLK and CLEAR, and 8 Product Terms available for the general data array (see Figure 3).

The basic macrocell architecture of the 5AC312 includes a user-programmable AND array and a user-configurable OR array. The inputs to the programmable AND array originate from the true and complement signals from the programmable input structure, the dedicated inputs, and the 24 feedback paths from the 12 I/O macrocells.

Programmable Input Structure

Figure 4 shows a block diagram of the 5AC312 input architecture. This device contains 8 user-program-

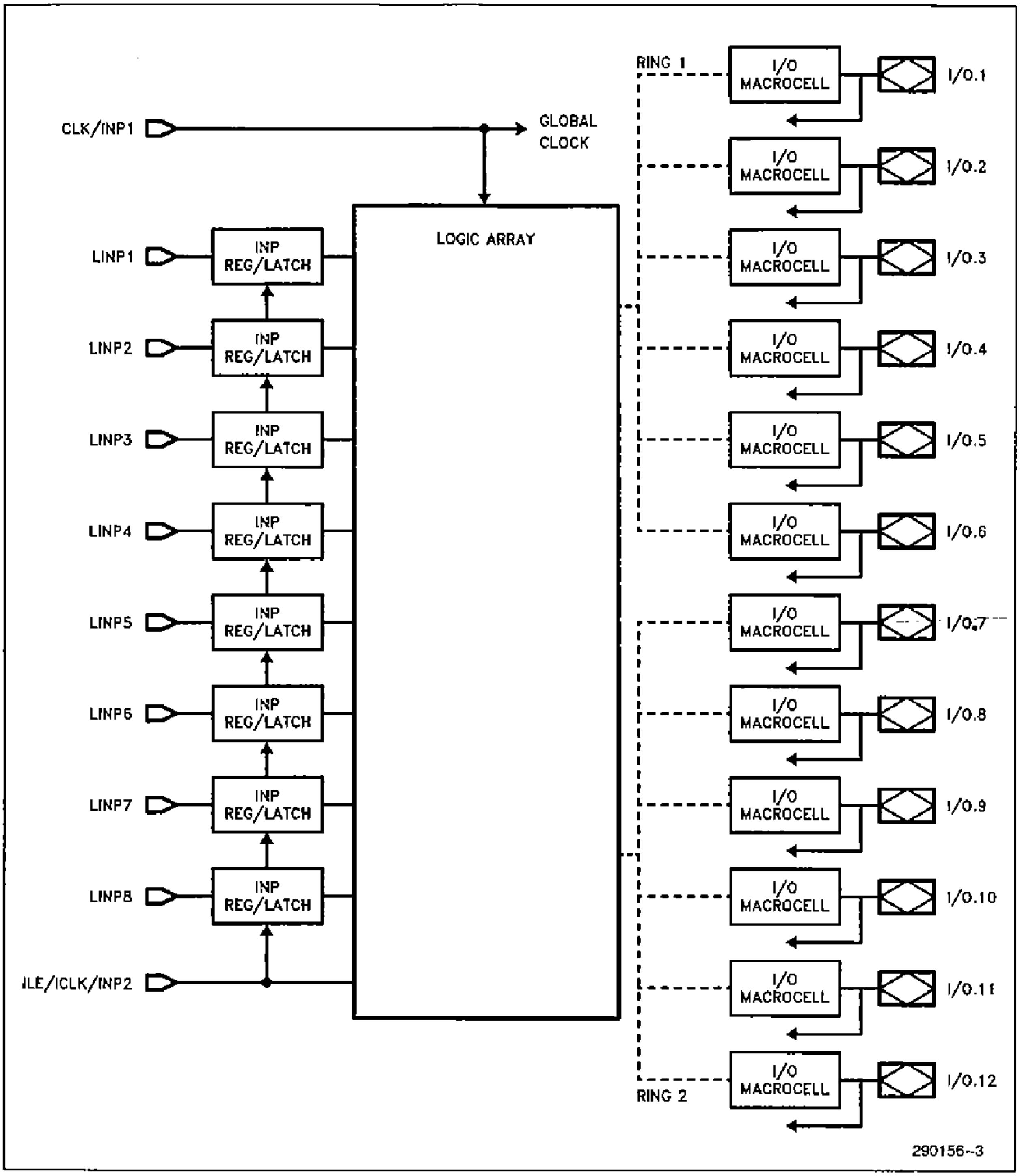


Figure 2. 5AC312 Architecture

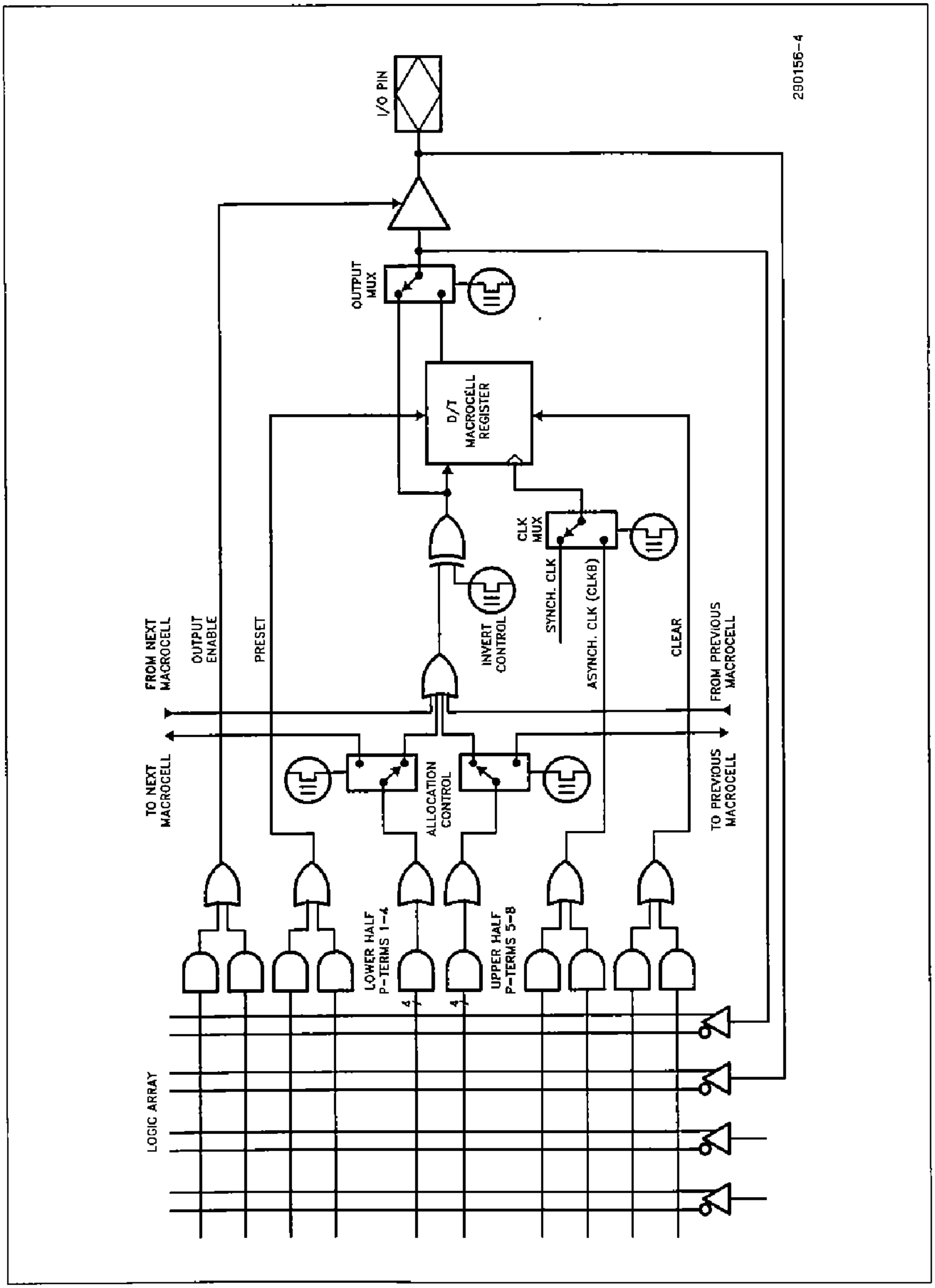
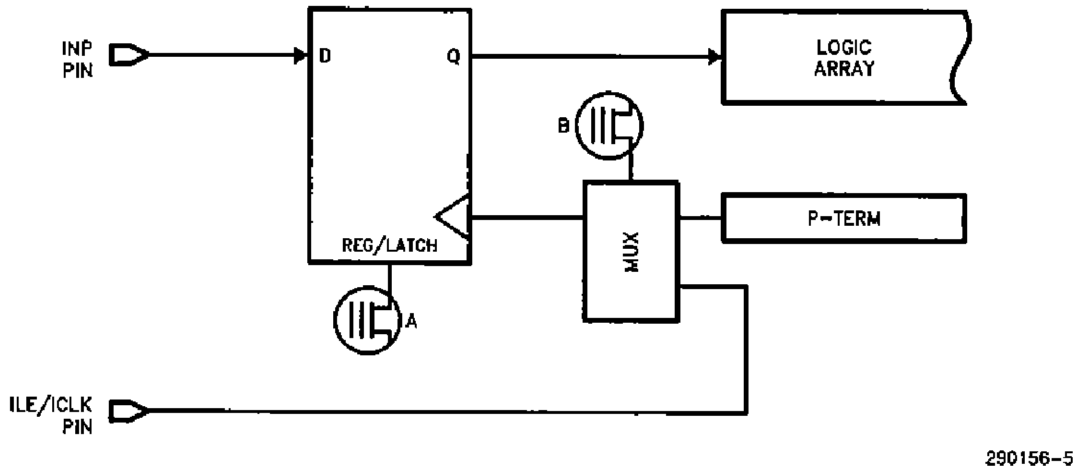


Figure 3. 5AC312 Basic Macrocell Structure



NOTE:
Flow-through input selected by connecting ILE P-Term to V_{CC}.

Figure 4. 5AC312 Input Structure

mable input structures that can be individually configured to work in one of five modes:

— Input register (D-register), synchronous operation
— Input register (D-register), asynchronous operation
— Input latch (D-latch), synchronous operation
— Input latch (D-latch), asynchronous operation
— Flow-through input

The configuration is accomplished through the programming of EPROM architecture control bits by the logic compiler and programmer software. If synchronous operation is chosen, the ILE/ICLK/INP becomes an ILE/ICLK (Input Latch Enable) input global to all input latch/register structures. For asynchronous operation, ILE/ICLK/INP can be used as a normal input (flow-through input) to the device while a separate Product Term in the control array is used to derive an input clock signal for the input structure. Because the clock signal for each input structure can be individually selected, a mix between synchronously and asynchronously clocked input structures is also possible.

Table 1 shows the input latch/register function table with respect to the synchronous ILE/ICLK input.

Table 1. 5AC312 Input Latch/Register Functions

Input Type	ILE/ICLK	D	Q
Latch	H	H	H
Latch	H	L	L
Latch	L	X	Qn
D-FF	↓	H	H
D-FF	↓	L	L
Flow-Through	X	H	H
Flow-Through	X	L	L

H = HIGH Level L = LOW Level X = Don't Care

Macrocell Array

Each of 12 macrocells in the 5AC312 contains 8 p-terms (Product Terms) to support logic functions. These 8 p-terms are subdivided into 2 groups each containing 4 p-terms. This grouping of p-terms supports the proprietary p-term allocation scheme.

Each macrocell can be configured as a D, T, RS, or JK register. The 8 p-terms for control functions are organized so that 2 p-terms support *each of the four* control signals. Control signals in the 5AC312 are: Output Enable (OE), asynchronous I/O register preset (PRESET), asynchronous clock for I/O registers (ASYNCH. CLK), and asynchronous I/O register reset (CLEAR).

CLK is a global clock signal that can be used to synchronously clock any or all macrocell registers. It can be used as an input to the logic array at the same time as a macrocell clock. When CLK is not used as a synchronous clock, it functions only as a dedicated input to the logic array.

Combinatorial Configuration

The macrocell register can be bypassed to implement combinatorial logic functions. When configured to provide combinatorial logic, only the OE control signal is used.

Invert Select Bit

An invert select EPROM bit is used to invert the product term input into each macrocell register, including double inputs on JK and SR registers. This invert option allows the highest possible logic utilization by use of DeMorgan's logic inversion.

LOGIC ARRAY

Each intersecting point in the logic array contains a programmable EPROM connection. Initially (erased state), all connections are complete, i.e., both true and complement states of all signals are connected to each p-term.

Connections are opened during programming. When both the true and complement connections exist, a logical false results on the output of the AND gate. If both the true and complement connections of a signal are programmed "open", then a logic "don't care" results for that signal. If all connections for a p-term are programmed open, then a logical true results on the output of the AND gate.

PRODUCT TERM ALLOCATION

Product Term allocation is defined as taking logic resources (p-terms) away from macrocells where they are not used to support demand for more than 8 Product Terms in other areas of the chip. In the 5AC312, this allocation can occur in increments of 4 p-terms between adjacent macrocells.

The 12 macrocells available in the 5AC312 are grouped into two "rings" with 6 macrocells per ring. Product Terms can be allocated in a "shift register" mode inside a ring; allocation of Product Terms between the rings is not supported. The two rings are shown in Figure 2 and listed in Table 2.

Example:

The logic function in macrocell 4 requires 16 p-terms. In this case, the iPLS II software allocates 4 p-terms from the previous macrocell in Ring 1 (macrocell 3) and 4 p-terms from the next macrocell in Ring 1 (macrocell 5) to accumulate a total of 16 p-terms (8 + 4 + 4). This implementation leaves macrocells 3 and 5 with a remainder of 4 p-terms each. These remaining p-terms in macrocells 3 and 5 can also be allocated away to or can be supplemented with p-terms from their respective previous/next macrocells in Ring 1.

Applying this scheme to the 5AC312 it becomes clear that any macrocell inside the device can support logic functions requiring between 0 and 16 Product Terms. Product Terms allocated away from a macrocell do not affect that macrocell's output structure. If all Product Terms are allocated "away" from a macrocell, the input to that macrocell's I/O control block is tied to GND. This polarity can be changed by programming the invert select EPROM bit. The I/O register as well as all secondary controls to this I/O control block are still available and can be used if needed.

The Product Term allocation scheme described above is automatically supported by iPLDS II V2.0 and is transparent to the user. Users can still use explicit pin assignments, but should assign pins in a way that does not conflict with p-term allocation.

Table 2. Product Term Allocation Rings

Ring 1			Ring 2		
Current Macro-cell	Next Macro-cell	Previous Macro-cell	Current Macro-cell	Next Macro-cell	Previous Macro-cell
1	2	6	7	8	12
2	3	1	8	9	7
3	4	2	9	10	8
4	5	3	10	11	9
5	6	4	11	12	10
6	1	5	12	7	11

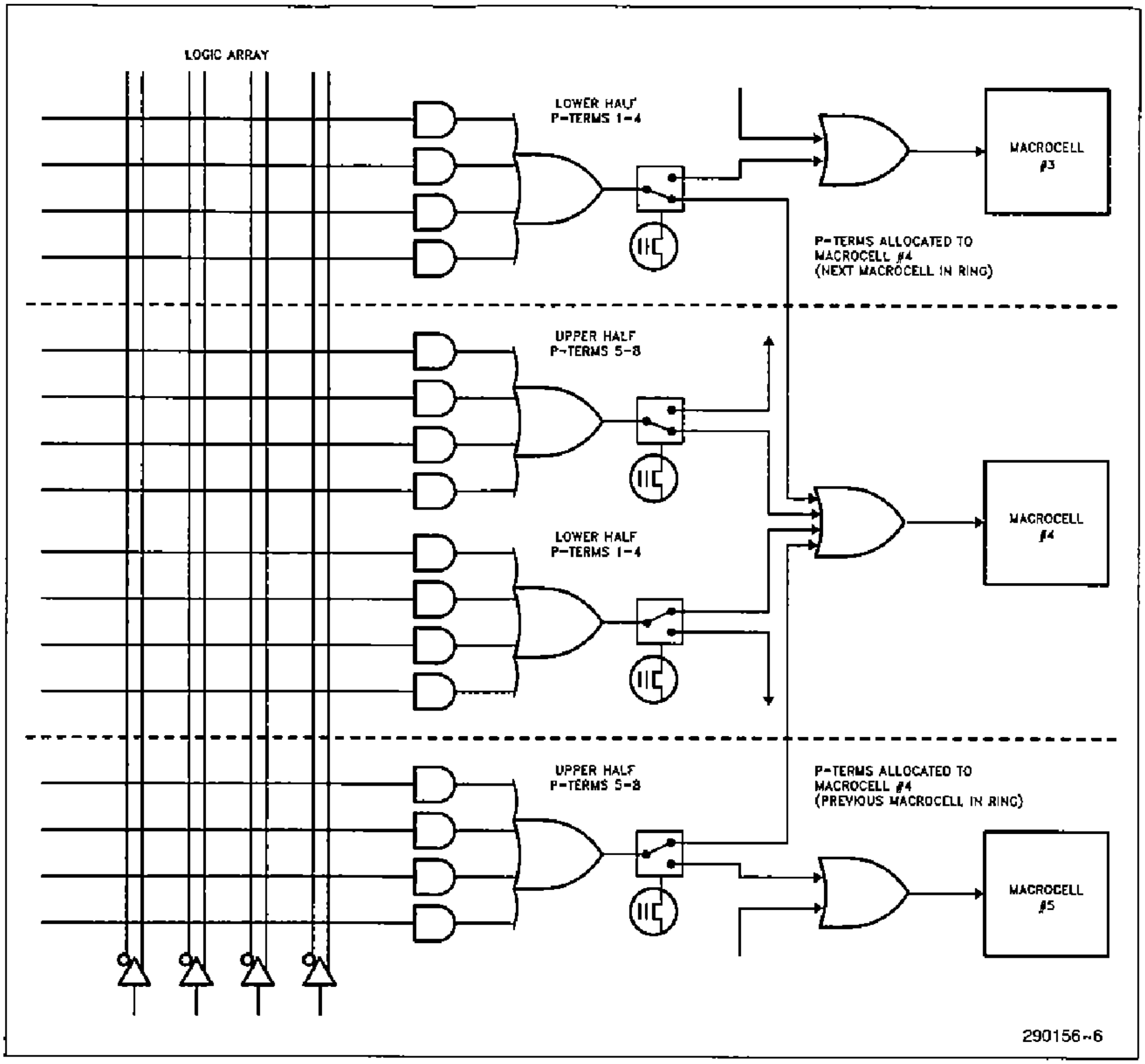


Figure 5. Product Term Allocation (8 + 4 + 4)

Macrocell I/O Control Block

Each macrocell in the 5AC312 has the ability to implement D, T, SR, and JK registered outputs as well as combinatorial outputs. The asynchronous set and reset inputs to each macrocell register allows implementation of true SR Flip-Flops. Registered outputs may be clocked from the synchronous CLK/INP1 pin or asynchronously clocked by the 2 Product Terms available for ASYNCH. CLK. The 5AC312 also features separate input and feedback paths (dual feedback) on all macrocell I/O control blocks. This enables the designer to utilize input pins when the associated macrocells have been assigned a no output with buried feedback attribute. Multiplexed I/O is accomplished by controlling the output buffer associated with each macrocell using the 2 Product Terms set aside for implementing an OE function.

DUAL-FEEDBACK/BURIED LOGIC

Macrocell output can be fed back to the logic array on either one of the two feedback paths. If the pin feedback is used (connected after the output buffer), bidirectional I/O can be implemented. If the internal feedback path is used to implement a buried register or buried logic function, the pin feedback is still available for use as an input. The availability of dual feedbacks on the 5AC312 enhances resource efficiency over single feedback devices.

Automatic Standby Mode

The 5AC312 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 20 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasuro, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

POWER-ON CHARACTERISTICS

The Macrocell registers of the 5AC312 will experience a reset to their inactive state (logic low) upon V_{CC} power-up. Using the PRESET function available to each macrocell, any particular register preset can be achieved after power-up. 5AC312 inputs and outputs begin responding within 10 μs (6 μs typical) after V_{CC} power-up or after a power-loss/power-up sequence. Input registers are not reset on power-up and are indeterminate. Input latches reflect the state of the input pins on power-up.

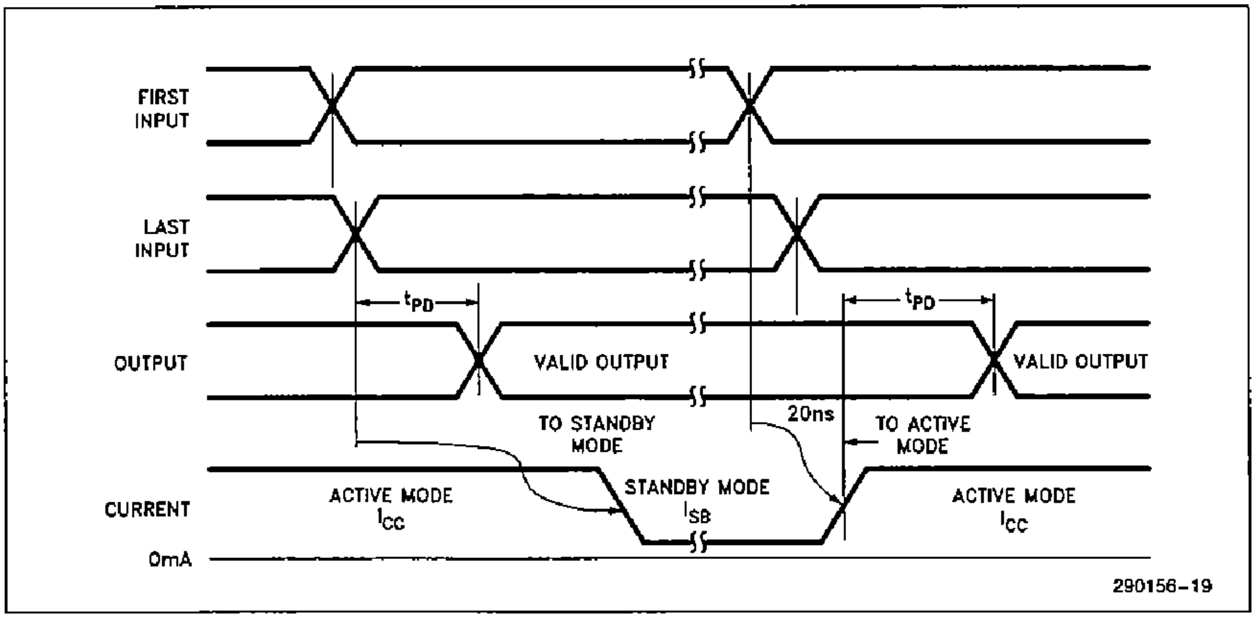


Figure 6. 5AC312 Standby and Active Mode Transitions

ERASED STATE CONFIGURATION

After erasure and prior to programming, all macrocells are configured as combinatorial, inverted outputs with output buffers three-stated. Inputs are configured as synchronous registers.

ERASURE CHARACTERISTICS

Erasure time for the 5AC312 is 1 hour at 12,000 μW/cm^2 with a 2537Å UV lamp.

Erasure characteristics of the device are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 5AC312 in approximately six years, while it would take approximately two weeks to erase the device when exposed to direct sunlight. If the device is to be exposed to these lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 5AC312 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of forty (40) Wsec/cm^2.

The erasure time with this dosage is approximately 1 hour using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during exposure. The maximum integrated dose the 5AC312 can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

int$_e$ligent Programming™ Algorithm

The 5AC312 supports the int$_e$ligent Programming algorithm which rapidly programs Intel H-EPLDs, EPROMs and Microcontrollers while maintaining a high degree of reliability. It is particularly suited for production programming environments. This method greatly decreases the overall programming time while programming reliability is ensured as the incremental program margin of each bit has been verified in the programming process. (Programming information for the 5AC312 is available from Intel by request.)

DESIGN SECURITY

A Security Bit provides a programmable security option to protect the data programmed in the device. Once this bit is set during programming, subsequent attempts to read the device architecture information are prevented. This method provides a higher degree of design security than fuse-based devices, since programmed EPROM cells are invisible even to microscopic examination. The Security Bit (also called the Verify Protect Bit), along with all the other EPROM cells, is reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the device have been designed to resist latch-up which is inherent in inferior CMOS structures. The 5AC312 is designed with Intel's proprietary 1-micron CHMOS EPROM process. Thus, each of the pins will not experience latch-up with currents up to 100 mA and voltages ranging from −0.5V to (V_{CC} + 0.5V). The programming pin is designed to resist latch-up to the 13.5 maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range (GND < (V_{IN} or V_{OUT}) < V_{CC}. All unused inputs and I/Os should be tied to V_{CC} or GND to minimize power consumption (do not leave them floating). A power supply decoupling capacitor of at least 0.2 μF must be connected directly between each V_{CC} and GND pin.

As with all CMOS devices, ESD handling procedures should be used with the 5AC312 to prevent damage to the device during programming, assembly, and test.

FUNCTIONAL TESTING

Since the logical operation of the 5AC312 is controlled by EPROM elements, the device is completely testable during the manufacturing process. Each programmable EPROM bit controlling the internal logic is tested using application-independent test patterns. EPROM cells in the 5AC312 are 100% tested for programming and erase. After testing, the devices are erased before shipments to the customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices are important features over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure device functionality. During the manufacturing process, tests on these parts can only be performed in very restricted manners to prevent pre-programming of the array.

INTEL PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM II (iPLDS II)

Release 2.0 (or later) of iPLDS II provides all the tools needed to design with the 5AC312 EPLD. In addition to providing development assistance, iPLDS II insulates the user from knowing the intricate details of EPLD architecture (the machine will optimize a design to benefit from architectural features). It contains comprehensive third generation software that supports four different design entry methods, minimizes logic, does automatic pin assignments and produces the best design fit for the selected EPLD. It is user friendly with guided menus, on-line Help messages and soft key inputs.

In addition, iPLDS II contains programmer hardware in the form of an iUP-PC Universal Programmer-Personal Computer to enable the user to program EPLDs, read and verify programmed devices and also to graphically edit programming files. The software generates industry standard JEDEC object code output files which can be downloaded to other programmers as well.

iPLS II software interfaces to several schematic capture packages to enable designs to be entered in schematic form. IPLDview-286/IPLDdraw allows the designer to use familiar TTL symbols or EPLD design primitive symbols. User-defined symbols are also supported. These products also provide a path to A.C. timing simulation of EPLD designs.

SCHEMA II-PLD allows the designer to use TTL symbols, EPLD custom macros, or EPLD design primitive symbols. It also supports user-defined symbols.

Other design formats include Boolean equation entry (supported directly by iPLS II) and state machine entry (supported by iSTATE).

iPLDS operates on the IBM† PC/XT, PC/AT, or other compatible machine with the following configuration:

1. At least one floppy disk drive and hard disk drive.
2. MS-DOS†† Operating System Version 3.0 or greater.
3. 512K Memory (640K recommended).
4. Intel iUP-PC Universal Programmer-Personal Computer and GUPI Adaptor (GUPI Adaptor ordered separately).
5. A color monitor is suggested.

Detailed information on the Intel Programmable Logic Development System II is contained in a separate Intel data sheet. (Order Number: 280168). Refer to the tools section of the *Programmable Logic* handbook for a complete listing of development tools.

†IBM Personal Computer is a registered trademark of International Business Machines Corporation.

††MS-DOS is a registered trademark of Microsoft Corporation.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	NOTF
LINP	JOJF
RINP	JONF
CONF	SONF
COCF	SOSF
COIF	TOIF
RONF	TONF
ROIF	TOTF
RORF	CLKB
NOCF	LINB
NORF	
NOJF	
NOSF	

ORDERING INFORMATION

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Order Code	Package	Operating Range
25	15	50	D5AC312-25	CERDIP	Commercial
			P5AC312-25	PDIP	
			N5AC312-25	PLCC	
30	18	40	D5AC312-30	CERDIP	Commercial
			P5AC312-30	PDIP	
			N5AC312-30	PLCC	

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC}) (1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP}) (1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb}) (3) .. −10°C to +85°C

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended temperature range versions are available.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

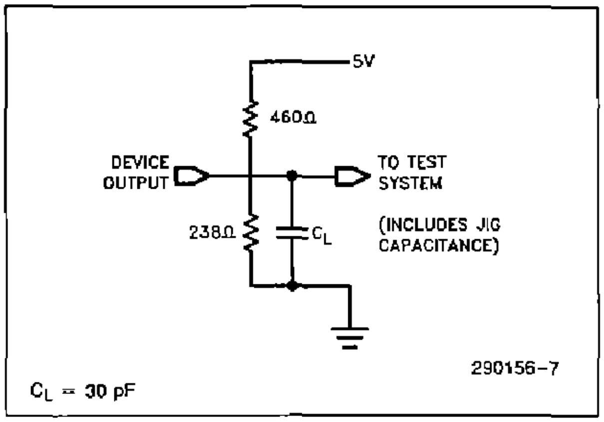
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}(5)	High Level Output Voltage	2.4			V	I_O = −4.0 mA D.C., V_{CC} = min.
V_{OL}	Low Level Output Voltage			0.45	V	I_O = 8.0 mA D.C., V_{CC} = min.
I_I	Input Leakage Current			±10	μA	V_{CC} = max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			±10	μA	V_{CC} = max., GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−90	mA	V_{CC} = max., V_{OUT} = 0.5V
I_{SB}(7)	Standby Current		100	150	μA	V_{CC} = max., V_{IN} = V_{CC} or GND, Standby Mode
I_{CC}(8)	Power Supply Current		10		mA	V_{CC} = max., V_{IN} = V_{CC} or GND, No Load, Input Freq. = 1 MHz Active Mode (Turbo = Off), Device Prog. as 12-Bit Ctr.

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included. Do not attempt to test these values without suitable equipment.
5. I_O at CMOS levels (3.84V) = −2 mA.
6. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
7. With Turbo Bit Off, device automatically enters standby mode approximately 100 ns after last input transition.
8. See graph at end of data sheet for I_{CC} vs. frequency.

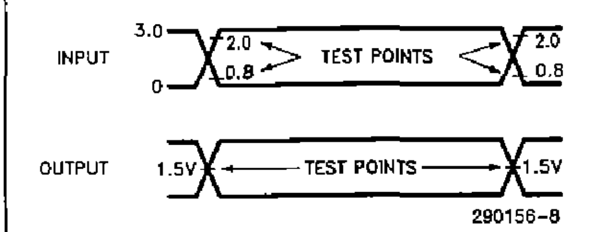
CAPACITANCE

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance			8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{OUT}	I/O Capacitance			15	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	ILE/ICLK/INP2 Capacitance			12	pF	V_{IN} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin (CLK/INP1)			25	pF	V_{IN} = 0V, f = 1.0 MHz

A.C. TESTING LOAD CIRCUIT



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. *Device input rise and fall times < 6 ns.*

A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit "On"(9)

Symbol	From	To	5AC312-25			5AC312-30			Non-(11) Turbo Mode	Unit
			Min	Typ	Max	Min	Typ	Max		
t_{PD1}	Input	Comb. Output		20	25		25	30	+20	ns
t_{PD2}	I/O	Comb. Output		20	25		25	30	+20	ns
t_{PZX}(10)	I or I/O	Output Enable		20	25		25	30	+20	ns
t_{PXZ}(10)	I or I/O	Output Disable		20	25		25	30	+20	ns
t_{CLR}	Asynch. Reset	Q Reset		20	25		25	30	+20	ns
t_{SET}	Asynch. Set	Q Set		20	25		25	30	+20	ns

NOTES:
9. Typical values are at T_A = 25°C, V_{CC} = 5V, Active Mode.
10. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady-state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF.
11. If device is operated with Turbo Bit Off (Non-Turbo Mode) and the device has been inactive for approximately 100 ns, increase time by amount shown.

SYNCHRONOUS CLOCK MODE (MACROCELLS) A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(11) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Max. Frequency (Pipelined) $1/t_{SU}$—No Feedback		66	50		50	40		MHz
f_{CNT}	Max. Count Frequency $1/t_{CNT}$—with Feedback		40	33		35	30		MHz
t_{SU1}	Input Setup Time to CLK	20	15		24	20		+20	ns
t_{SU2}	I/O Setup Time to CLK	20	15		24	20		+20	ns
t_H	I or I/O Hold after CLK High	0			0				ns
t_{CO}	CLK High to Output Valid		10	15		12	18		ns
t_{CNT}	Macrocell Output Feedback to Macrocell Input—Internal Path	30	25		35	30		+20	ns
t_{CH}	CLK High Time	10			12.5				ns
t_{CL}	CLK Low Time	10			12.5				ns

SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE) A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(11) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
f_{MAXI}	Max. Frequency		50	40		40	33		MHz
t_{SUIR}	Input Register/Latch Setup Time before ILE/ICLK	5			5				ns
t_{PLI}(12)	Minimum Input Clock Period		20	25		25	30	+20	ns
t_{HI}	I Hold after ICLK/ILE ↓	7			10				ns
t_{COI}	ICLK ↓ to Comb. Output		30	35		35	40	+20	ns
t_{EOI}	ILE ↑ to Comb. Output		30	35		35	40	+20	ns
t_{CHI}	ILE/ICLK High Time	10			12.5				ns
t_{CLI}	ILE/ICLK Low Time	10			12.5				ns

NOTE:

12. t_{PLI} = Input signal through registers/latch to macrocell register input.

ASYNCHRONOUS CLOCK MODE A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(11) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
INPUT STRUCTURE									
f_{AMAXI}	Max. Frequency Input Register $1/(t_{ACLI} + t_{ACHI})$			50			40		MHz
t_{ASUI}	Input Register/Latch Setup Time to Asynch. ILE/ICLK	0			0				ns
t_{AHI}	Input Register/Latch Hold after Asynch. ILE/ICLK	20	14		25	20		+20	ns
t_{ACOI}	Asynch. ICLK to Comb. Output		40	48		45	55	+20	ns
t_{AEOI}	Asynch. ILE ↑ to Comb. Output		40	48		45	55	+20	ns
t_{ACHI}	Asynch. ICLK High Time	10			12.5			+20	ns
t_{ACLI}	Asynch. ICLK Low Time	10			12.5			+20	ns
MACROCELLS									
f_{AMAX}	Max. Frequency (Pipelined) $1/(t_{ACL} + t_{ACH})$—No Feedback			50			40		MHz
f_{ACNT}	Max. Frequency $1/t_{ACNT}$—with Feedback		40	33		35	30		MHz
t_{ASU1}	Input Setup Time to Asynch. Clock	10			12			+20	ns
t_{ASU2}	I/O Setup Time to Asynch. Clock	10			12			+20	ns
t_{AH}	Input or I/O Hold after Asynch. Clock	5	0		5	0			ns
t_{ACO}	Asynch. CLK to Output Valid		20	25		25	30	+20	ns
t_{ACNT}	Register Output Feedback to Register Input—Internal Path	30	25		35	30		+20	ns
t_{ACH}	Asynch. CLK High Time	10			12.5			+20	ns
t_{ACL}	Asynch. CLK Low Time	10			12.5			+20	ns

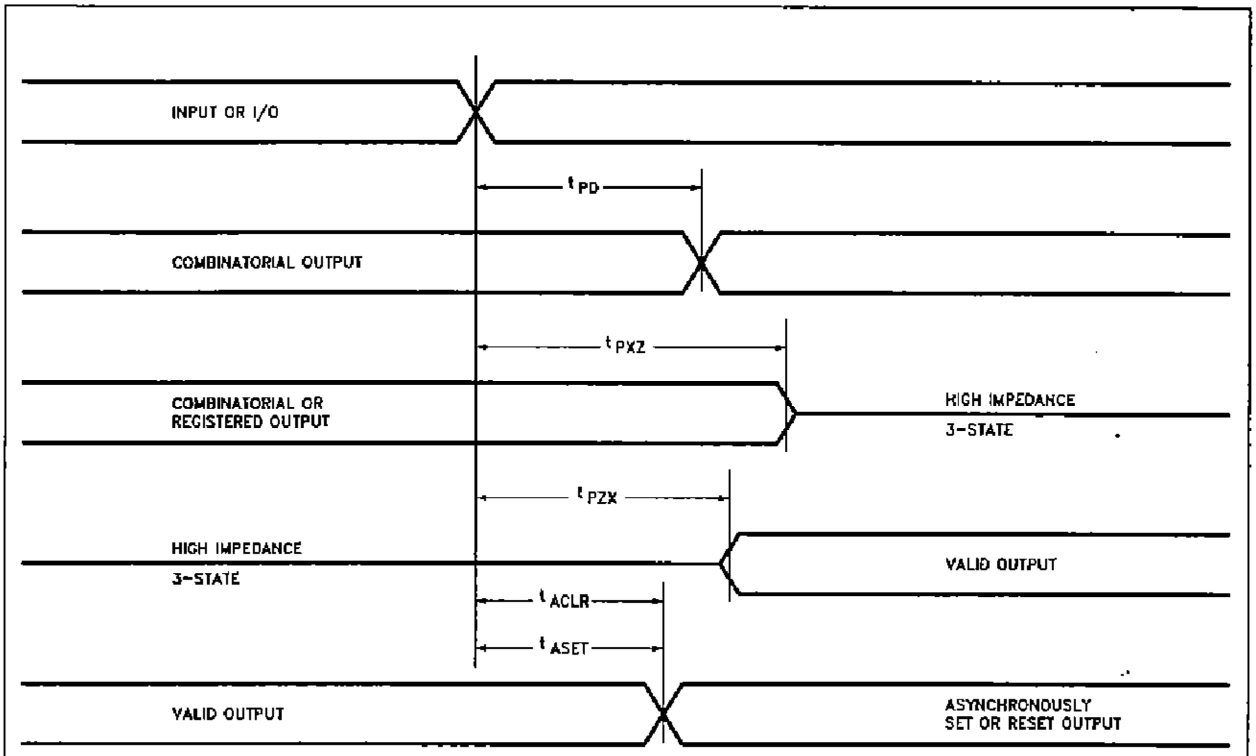
INPUT-CLOCK-TO-MACROCELL-CLOCK A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Turbo Bit On(8)

Symbol	Parameter	5AC312-25			5AC312-30			Non-(11) Turbo Mode	Unit
		Min	Typ	Max	Min	Typ	Max		
t_{C1C2}	Synchronous ILE/ICLK to Synchronous Macrocell CLK	25			30			+20	ns
	Synchronous ILE/ICLK to Asynchronous Macrocell CLK	15			18			+20	ns
	Asynchronous ILE/ICLK to Synchronous Macrocell CLK	35			40			+20	ns
	Asynchronous ILE/ICLK to Asynchronous Macrocell CLK	25			35			+20	ns

SWITCHING WAVEFORMS

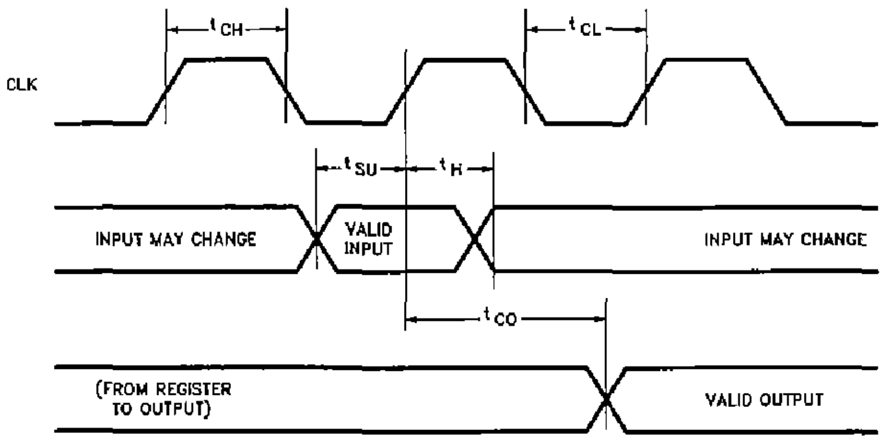
COMBINATORIAL MODE



290156-9

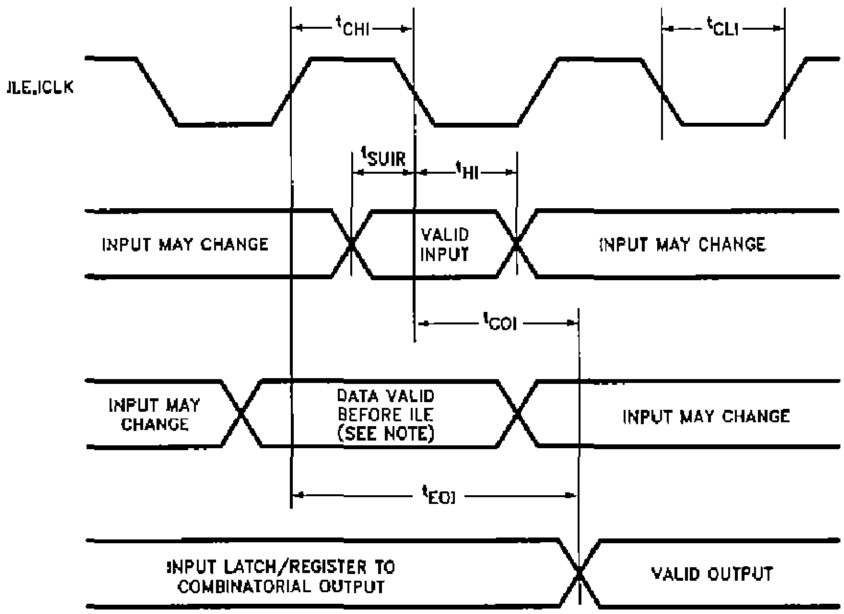
SWITCHING WAVEFORMS (Continued)

SYNCHRONOUS CLOCK MODE (MACROCELLS)



290156-10

SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)

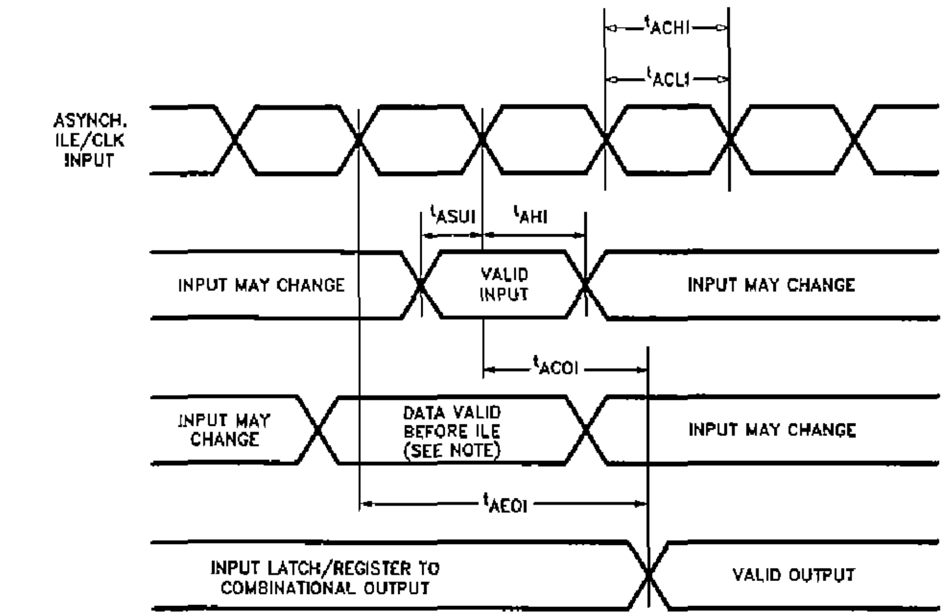


NOTE: WHEN ILE GOES HIGH BEFORE DATA IS VALID, USE t_{PD} INSTEAD OF t_{EOI}.

290156-11

SWITCHING WAVEFORMS (Continued)

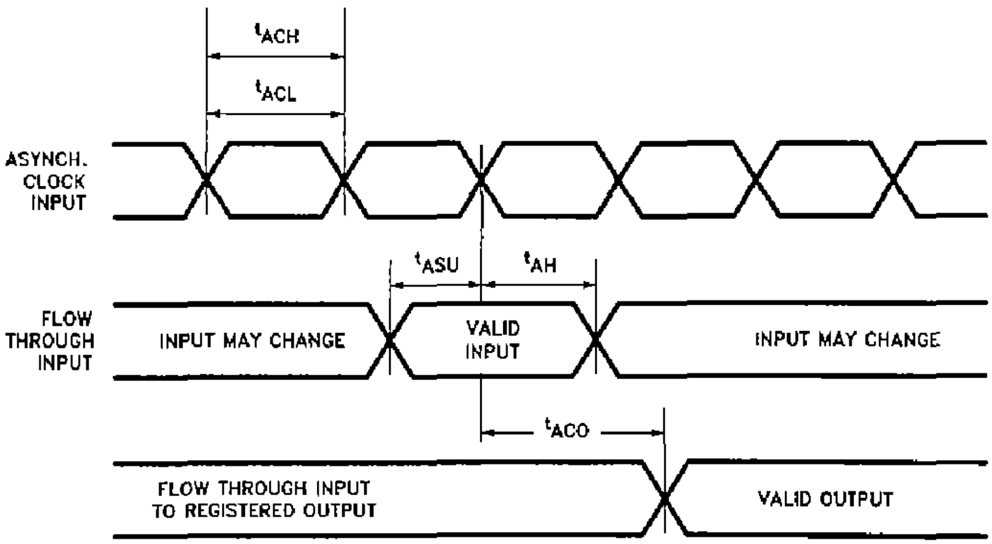
ASYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



NOTE: WHEN ILE GOES HIGH BEFORE DATA IS VALID, USE t_{PD} INSTEAD OF t_{AEOI}.

290156-13

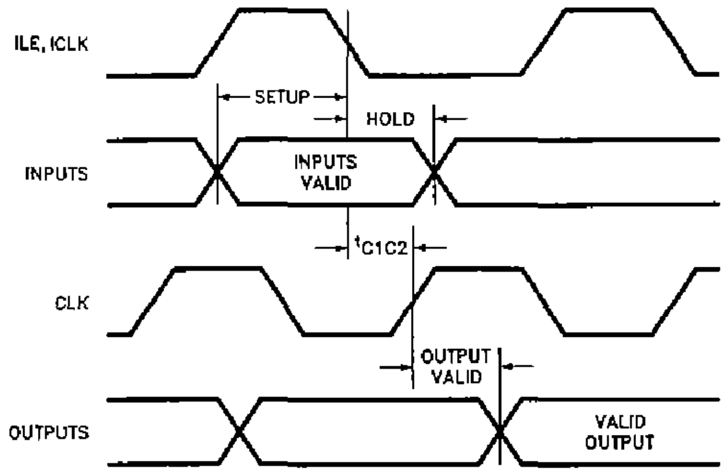
ASYNCHRONOUS CLOCK MODE (MACROCELLS)



290156-12

SWITCHING WAVEFORMS (Continued)

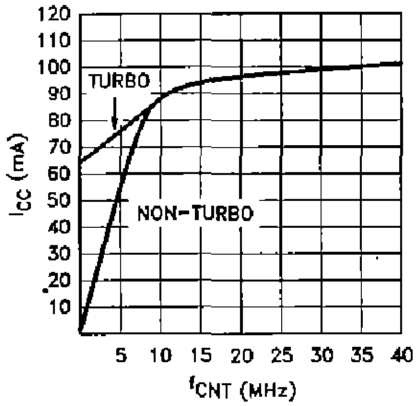
INPUT CLOCK-TO-MACROCELL CLOCK TIMING (CLOCKED PIPELINED DATA)



290156-18

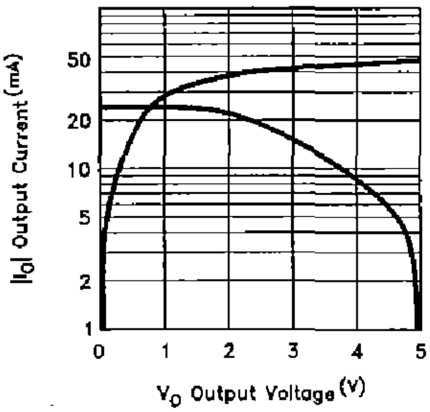
CLOCK, SETUP, HOLD, and OUTPUT VALID times are dependent on synchronous/asynchronous clocking and are listed in the specification tables.

Current in Relation to Frequency



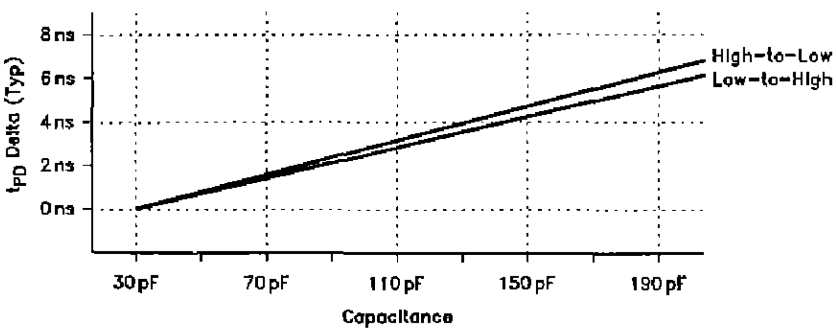
Conditions: $T_A = +25°C$, $V_{CC} = 5.25V$ 290156-20

Output Drive Current in Relation to Voltage



Conditions: $T_A = +25°C$ 290156-16

5AC312 t_{PD} vs Capacitive Loading



290156-21

$T_A = +25°C$
$V_{CC} = 5.0V$

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